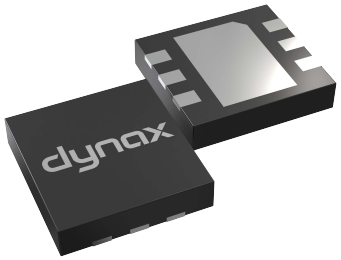
DXG2PH50A-90N

RF Power GaN Transistor



1. Product profile

1.1 General description

DXG2PH50A-90N is a 90 W RF GaN HEMT Transistor with second generation RF GaN technology from Dynax, which is ideal for cellular base station applications at frequencies from 4800 MHz to 5000 MHz.

Table 1. Typical performance [1]

Freq (MHz)	P_{sat} [2] (dBm)	P_{avg} [3] (dBm)	η_D [3] (%)	G_P [3] (dB)	ACPR [3] (dBc)
4800	49.7	41.3	48.0	12.3	-32.0
4880	49.6	41.3	48.3	12.5	-31.0
4960	49.5	41.3	49.2	12.3	-32.0

[1] Typical Doherty performance in Dynax Demo with the device soldered onto the heatsink, test condition: V_{DS} = 48 V, I_{DQA} = 60 mA , V_{GSB} = - 5.6 V.

[2] Test condition: Input signal Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[3] Test condition: Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF. ACPR measured in 3.84 MHz channel bandwidth @ ± 5 MHz offset.

1.2 Features and benefits

- High efficiency, high gain
- Internally matched for broadband performance
- Designed for Digital Pre-Distortion error correction systems
- Optimized for Doherty applications

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 4800 MHz to 5000 MHz frequency range

1.4 Lead-free and RoHS compliant

2. Pinning information

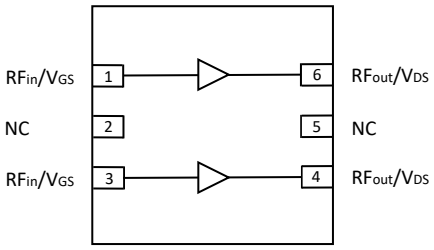


Fig 1. Pin configuration (Top view)

3. Ordering information

Table 2. Ordering information

Part number	Marking	Package type	Packaging information
DXG2PH50A-90N	DC9B	DFN 7×6.5mm	Tray: Suffix = 416 units
			Tape and Reel：Suffix = 1000 units；16 mm Tape width；13-inch Reel

4. Maximum ratings

Table 3. Maximum ratings

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	-10 ~ +2	V
Operating Voltage	V_{DS}	0 ~ +55	V
Maximum Forward Gate Current	I_{GMAX}	10.3	mA
Storage Temperature Range	T_{STG}	- 65 ~ +150	℃
Operating Junction Temperature	T_J	225	℃
Absolute Maximum Channel Temperature [1]	T_{MAX}	275	℃

[1] Functional operation above 225℃ has not been characterized and is not implied. Operation at T_{MAX} (275℃) reduces median time to failure by an order of magnitude; Operation beyond T_{MAX} could cause permanent damage.

5. Thermal characteristics

Table 4. Thermal characteristics

Parameter	Symbol	Value	Unit
Side A, Carrier			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 12.0 W	R_{thjc}(IR)	4.4	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 12.0 W	R_{thjc}(FEA)	6.5	℃/W
Side B, Peaking			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 3.0 W	R_{thjc}(IR)	2.3	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 3.0 W	R_{thjc}(FEA)	3.8	℃/W

6. Electrical characteristics (TA = 25℃ unless otherwise noted)

Table 5. DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Side A, Carrier					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	3.9	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 3.9 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 3.9 mA)	$V_{GS(th)}$	-4.0	-3.3	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 60 mA)	$V_{GS(Q)}$	-	-3.0	-	V
Side B, Peaking					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	6.4	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 6.4 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 6.4 mA)	$V_{GS(th)}$	-4.0	-3.3	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 90 mA)	$V_{GS(Q)}$	-	-3.0	-	V

7. Test information

7.1 Pulsed CW

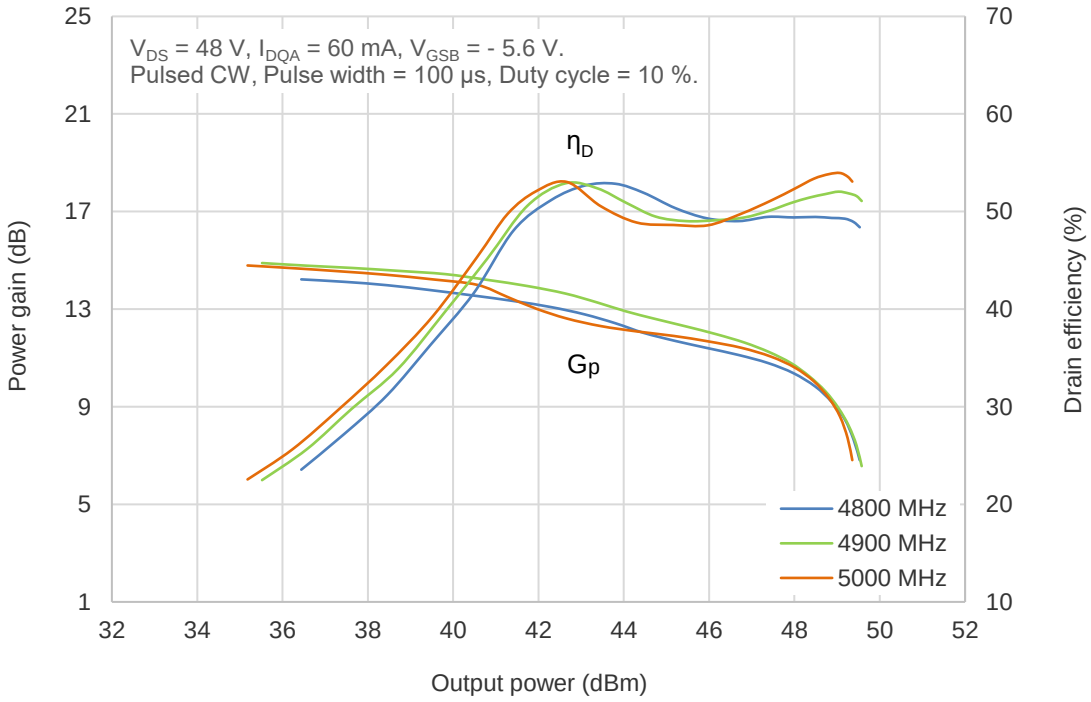


Fig 2. Power gain, Drain efficiency vs. Pulse output power

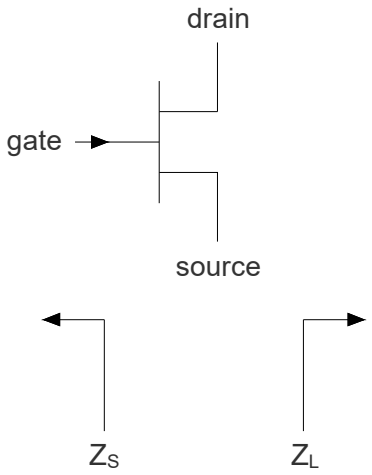


Fig 3. Definition of transistor impedance

8. Median lifetime

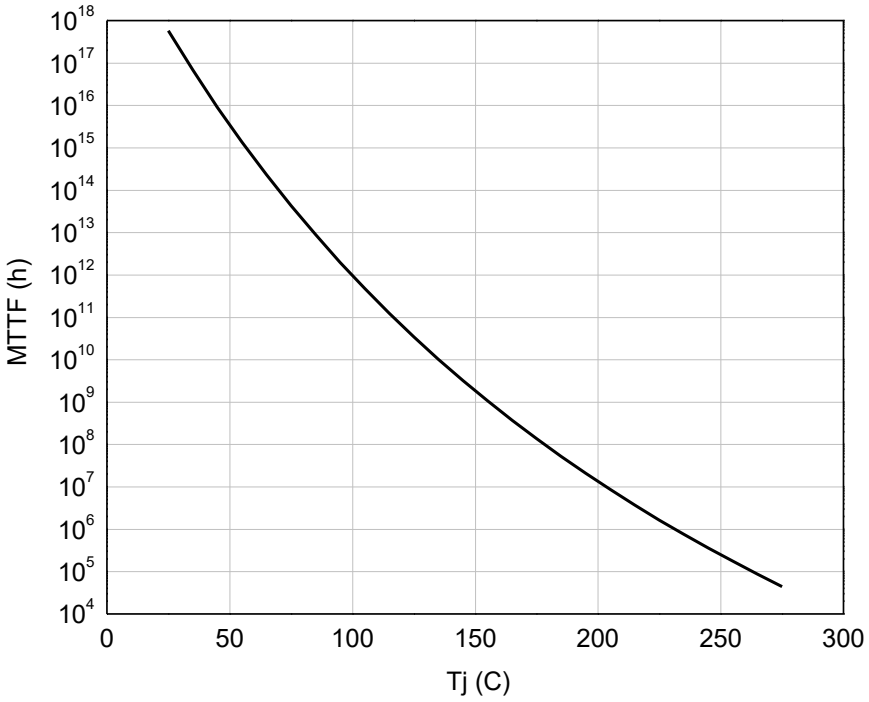


Fig 4. Median lifetime vs. channel temperature

9. Package outline

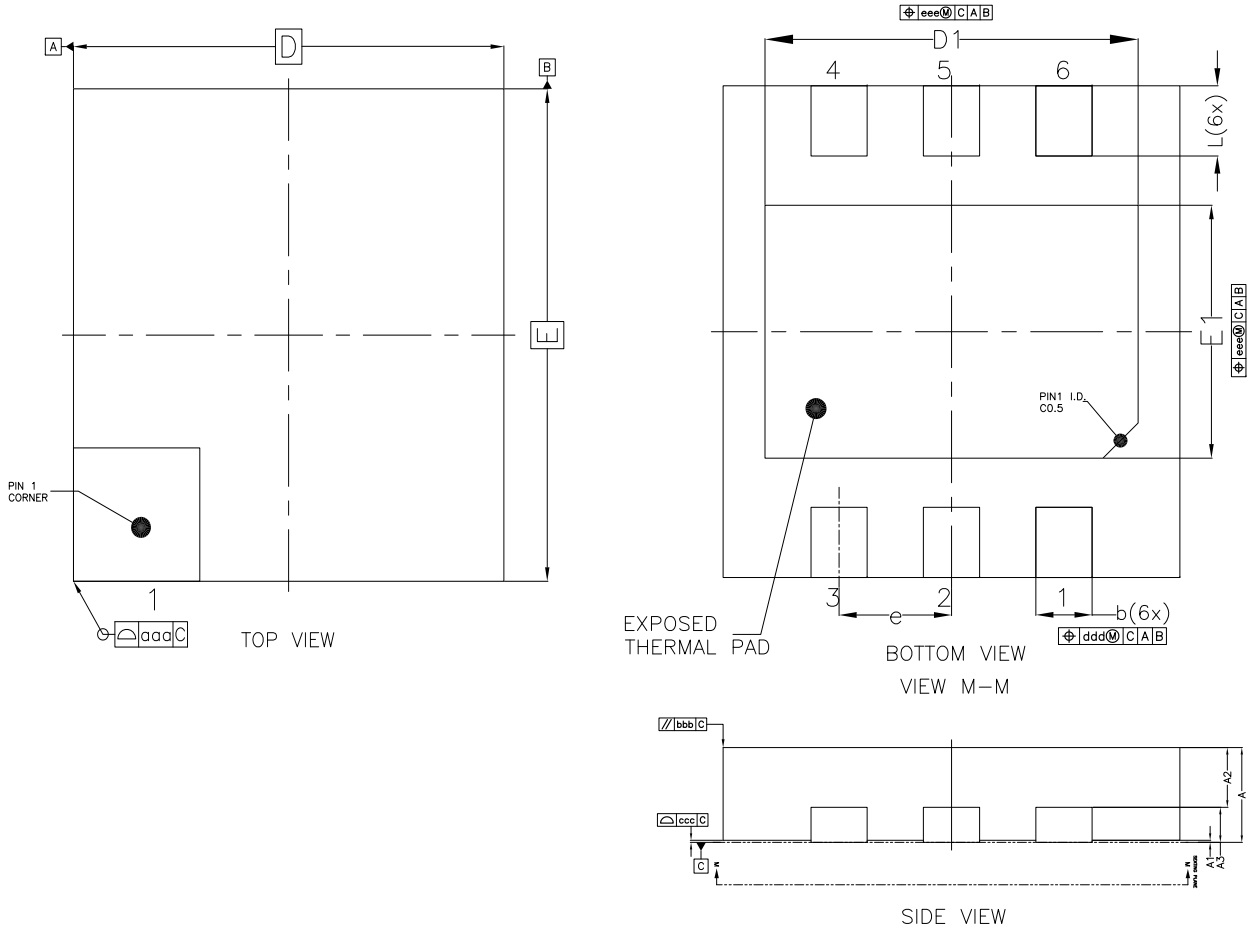


Fig 5. Package outline —— DFN 7×6.5mm

Table 6. Package dimensions

DESCRIPTION		DIM	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	1.30	1.35	1.43
STAND OFF		A1	0.00	-----	0.08
MOLD THICKNESS		A2	0.80	0.85	0.93
L/F THICKNESS		A3		0.50 REF	
BODY SIZE	X	D	6.43	6.50	6.60
	Y	E	6.93	7.00	7.10
LEAD PITCH		e		1.60 BSC	
LEAD WIDTH		b	0.75	0.80	0.88
LEAD LENGTH		L	0.95	1.00	1.08
EP SIZE		D1	5.26	5.31	5.39
		E1	3.55	3.60	3.68
Tolerance of form and position					
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	

(Continued)

DESCRIPTION	DIM	MILLIMETER		
		MIN	NOM	MAX
LEAD COPLANARITY	ccc		0.08	
LEAD POSITION OFFSET	ddd		0.1	
EXPOSED PAD OFFSET	eee		0.1	

10. Abbreviations

Table 7. Abbreviations

Acronym	Description
CW	Continuous Waveform
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing Wave Ratio

11. Legal information

11.1 Datasheet status

Document status	Product status	Definition
Objective [short] datasheet	Engineering sample	This document contains data from the objective specification for product development.
Preliminary [short] datasheet	Engineering sample	This document contains data from the preliminary specification.
Production [short] datasheet	Mass product	This document contains the product specification.

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