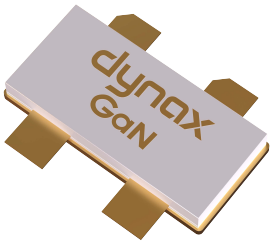
DXG1CH08A-540EF

RF Power GaN Transistor



1. Product profile

1.1 General description

DXG1CH08A-540EF is a 540 W RF GaN HEMT Transistor with first generation RF GaN technology from Dynax, which is ideal for cellular base station applications at frequencies from 758 MHz to 821 MHz.

Table 1. Typical performance

Freq (MHz)	P_{sat} [1] (dBm)	P_{avg} [2] (dBm)	η_D [2] (%)	G_P [2] (dB)	ACPR [2] (dBc)
758~803	57.0	49.0	58.0	18.0	-28.0

[1] Test condition: Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[2] Typical Doherty performance in Dynax Demo with the device soldered onto the heatsink, test condition: V_{DS} = 48 V, I_{DQA} = 500 mA, V_{GSB} = - 4.5 V, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF. ACPR measured in 3.84 MHz channel bandwidth @ ±5 MHz offset.

1.2 Features and benefits

- High efficiency, high gain
- Internally matched for broadband performance
- Designed for Digital Pre-Distortion error correction systems
- Optimized for Doherty applications

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 758 MHz to 821 MHz frequency range

1.4 Lead-free and RoHS compliant

Pb RoHS

2. Pinning information

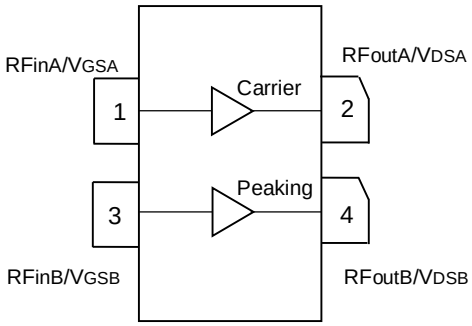


Fig 1. Pin configuration (Top view)

3. Ordering information

Table 2. Ordering information

Part number	Marking	Package type	Packaging information
DXG1CH08A-540EF	DXG1CH08A-540EF	780P2GB	Tray: Suffix = 20 units
			Tape and Reel: Suffix = 100 units; 44 mm Tape width; 13-inch Reel

4. Maximum ratings

Table 3. Maximum ratings

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	-10 ~ +2	V
Operating Voltage	V_{DS}	0 ~ +55	V
Maximum Forward Gate Current	I_{GMAX}	57.2	mA
Storage Temperature Range	T_{STG}	- 65 ~ +150	℃
Operating Junction Temperature	T_J	225	℃
Absolute Maximum Channel Temperature [1]	T_{MAX}	275	℃

[1] Functional operation above 225℃ has not been characterized and is not implied. Operation at T_{MAX} (275℃) reduces median time to failure by an order of magnitude; Operation beyond T_{MAX} could cause permanent damage.

5. Thermal characteristics

Table 4. Thermal characteristics

Parameter	Symbol	Value	Unit
Side A, Carrier			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 42.7 W	R_{thjc}(IR)	1.4	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 42.7 W	R_{thjc}(FEA)	1.8	℃/W
Side B, Peaking			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 10.7 W	R_{thjc}(IR)	0.9	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 10.7 W	R_{thjc}(FEA)	1.1	℃/W

6. ESD protection characteristics

Table 5. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2012)	1A (> 250 V)
Charged Device Model (per JESD22-C101F)	C2 (> 500 V)

7. Moisture sensitivity level

Table 6. Moisture sensitivity level

Test methodology	Class
Moisture Sensitivity Level (per J-STD-020)	Level 1

8. Electrical characteristics (TA = 25℃ unless otherwise noted)

Table 7. DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Side A, Carrier					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	22.0	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 22.0 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 22.0 mA)	$V_{GS(th)}$	-4.0	-3.2	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 500 mA)	$V_{GS(Q)}$	-	-3.0	-	V
Side B, Peaking					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	35.2	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 35.2 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 35.2 mA)	$V_{GS(th)}$	-4.0	-3.2	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 850 mA)	$V_{GS(Q)}$	-	-3.0	-	V

Table 8. RF characteristics (Typical Doherty performance – 803 MHz) [1]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Peak Output Power [2]	P_{sat}	55.7	56.7	-	dBm
Drain Efficiency [3]	η_D	53.8	60.8	-	%
Power Gain [3]	G_P	17.9	19.5	21.1	dB

[1] Typical Doherty performance in Dynax DXG1CH08A-540EF production test fixture, test condition: V_{DS} = 48 V, I_{DQA} = 250 mA, V_{GSB} = -2.0 V + V_{GSQ} @100 mA.

[2] Test condition: Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[3] Test condition: P_{avg} = 49.0 dBm, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF.

Table 9. Load mismatch

Parameter	Result
VSWR 10:1 at V_{DS} = 48 V, 500 W Pulsed CW output power, Pulse width = 100 µs, Duty cycle = 10%.	No device damage

9. Test information

9.1 Typical application circuit

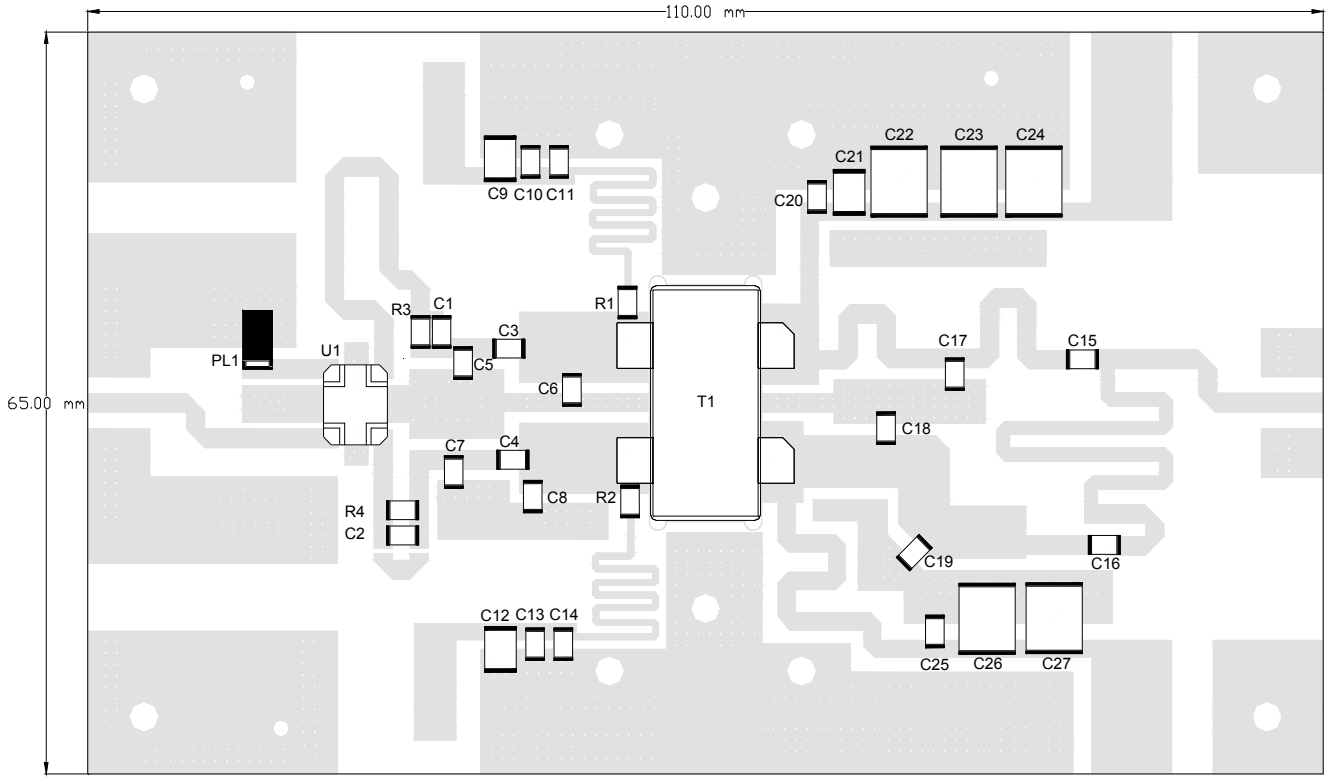


Fig 2. Component layout

Table 10. List of components

S/N	Type	Designator	Description	Value	Vendor
1	Cap	C1,C2,C15	ATC600F100JT250XT	10 pF	ATC
2	Cap	C3,C4,C11,C14,C20,C25	ATC600F680JT250XT	68 pF	ATC
3	Cap	C5	ATC600F6R8JT250XT	6.8 pF	ATC
4	Cap	C7	ATC600F5R6JT250XT	5.6 pF	ATC
5	Cap	C6,C8,C19	ATC600F8R2JT250XT	8.2 pF	ATC
6	Cap	C17	ATC100B4R7JT500XT	4.7 pF	ATC
7	Cap	C18	ATC600F4R3JT250XT	4.3 pF	ATC
8	Cap	C16	ATC100B220JT500XT	22 pF	ATC
9	Cap	C10,C13	CGA4J2X7R2A333KT0Y0U	33 nF	TDK
10	Cap	C9,C12,C21	GRM31CZ72A225KE	2.2 uF	Murata
11	Cap	C22,C23,C24,C26,C27	C5750X7S2A106KY000N	10 uF	TDK
12	Res	R1,R2	RC0805FR_0710RL	10 Ω	Yageo
13	Res	R3,R4	RC0805FR_0751RL	50 Ω	Yageo
14	Power load	PL1	SN1206	50 Ω	RN2
15	HyBrid coupler	U1	CMX21Q03	3 dB	RN2
16	Transistor	T1	DXG1CH08A-540EF	/	Dynax
17	PCB	/	Rogers4350	30 mil	Rogers

10. Impedance information

Table 11. Typical impedance of carrier [1]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
758	2.4 - j6.2	4.9 + j1.3	24.1	54.0	251	74.8
790	2.8 - j6.7	4.7 + j1.8	23.7	54.0	251	74.1
821	3.2 - j7.5	4.3 + j2.0	23.5	54.1	257	74.3
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
758	2.4 - j6.2	8.1 + j8.2	25.8	51.5	141	85.1
790	2.8 - j6.7	8.0 + j7.5	25.5	51.6	144	84.2
821	3.2 - j7.5	7.4 + j6.3	25.1	51.5	141	84.7

Table 12. Typical impedance of peaking [2]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
758	2.2 - j5.0	3.1 + j0.5	23.6	55.9	389	73.2
790	2.4 - j5.4	3.0 + j0.4	23.3	56.0	398	73.5
821	2.6 - j5.8	2.9 + j0.4	23.1	56.0	398	72.9
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
758	2.2 - j5.0	4.8 + j4.8	25.2	52.6	181	84.0
790	2.4 - j5.4	4.7 + j4.1	24.8	52.8	190	83.4
821	2.6 - j5.8	4.5 + j3.6	24.5	52.5	177	83.5

[1] V_{DS} = 48 V, I_{DQA} = 500 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

[2] V_{DS} = 48 V, I_{DQB} = 850 mA, Pulsed CW, Pulse width = 100 µs, Duty cycle = 10 %.

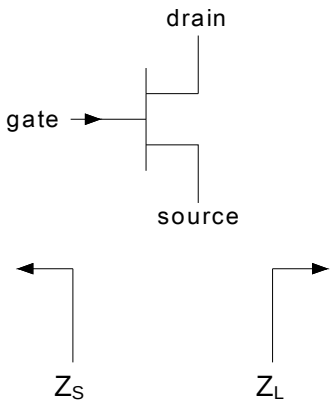


Fig 3. Definition of transistor impedance

11. Median lifetime

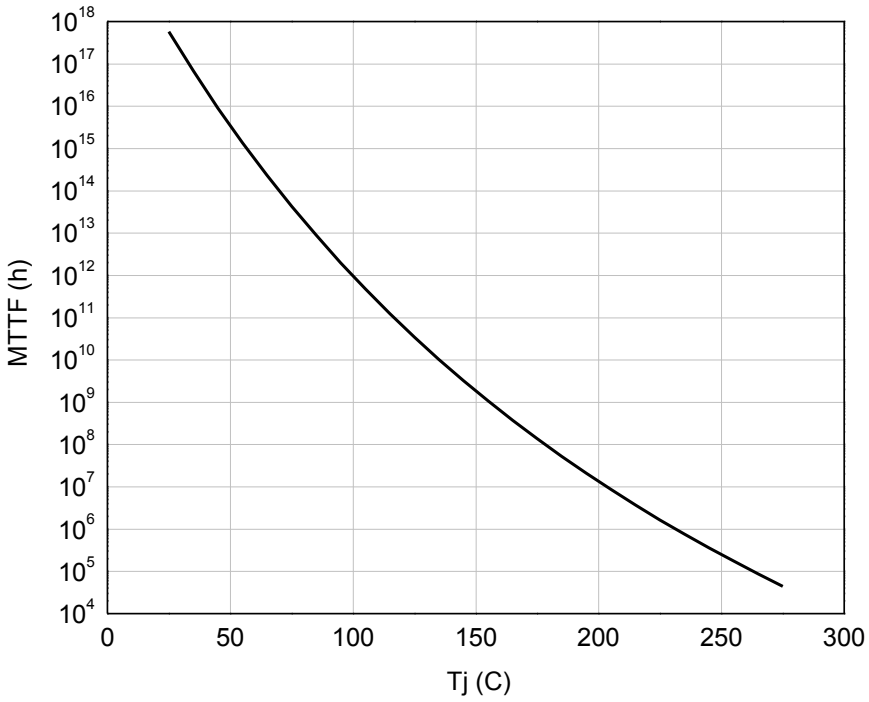
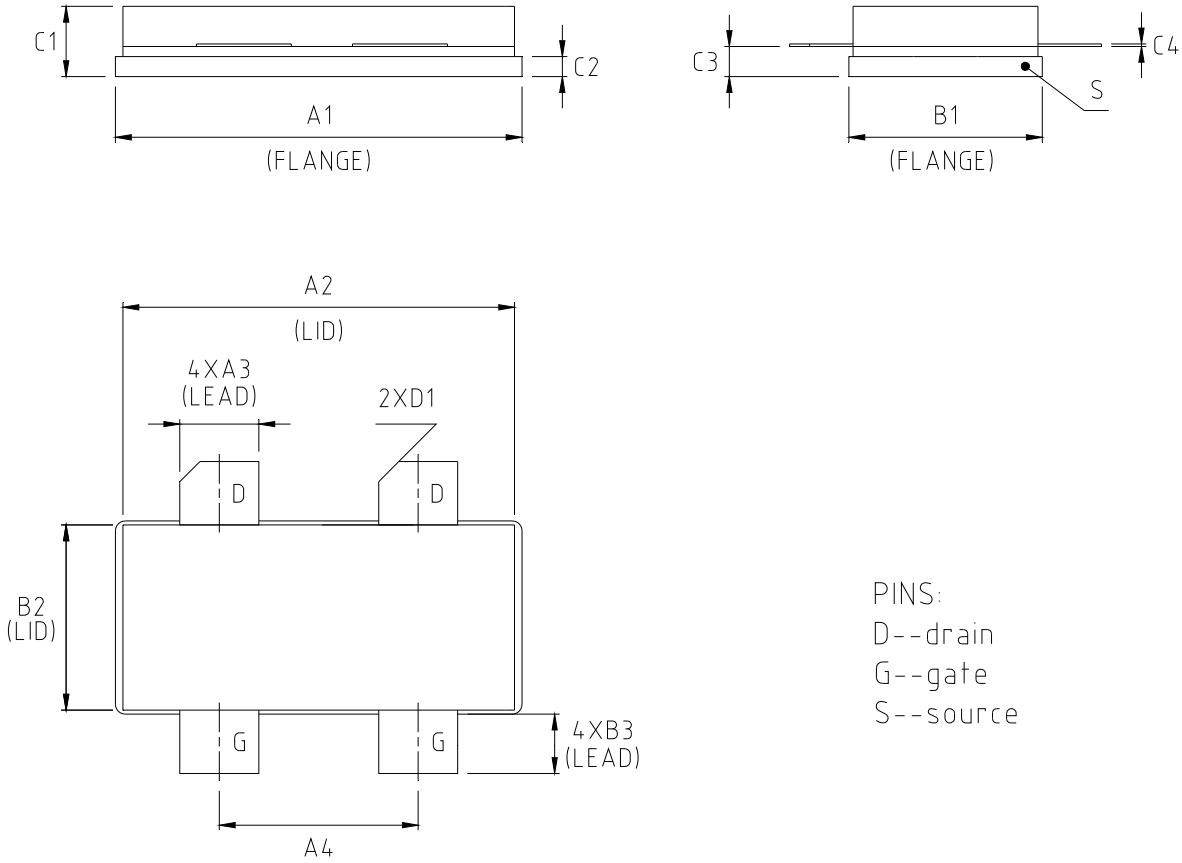


Fig 4. Median lifetime vs. channel temperature

12. Package outline



DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX
A1	0.805	0.815	20.45	20.70
A2	0.772	0.788	19.61	20.02
A3	0.153	0.162	3.87	4.13
A4	0.385	0.395	9.77	10.03
B1	0.380	0.390	9.65	9.91
B2	0.365	0.375	9.27	9.53
B3	0.108	0.128	2.75	3.25
C1	0.130	0.170	3.30	4.32
C2	0.035	0.045	0.89	1.14
C3	0.057	0.067	1.45	1.70
C4	0.003	0.006	0.08	0.15
D1	0.040 45°REF		1.02 45°REF	

Fig 5. Package outline —— 780P2GB

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	Electro-Static Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing Wave Ratio

14. Legal information

14.1 Datasheet status

Document status	Product status	Definition
Objective [short] datasheet	Engineering sample	This document contains data from the objective specification for product development.
Preliminary [short] datasheet	Engineering sample	This document contains data from the preliminary specification.
Production [short] datasheet	Mass product	This document contains the product specification.

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